REMARKS

The Examiner's Action mailed on October 10, 2007, has been received and its contents carefully considered.

Claims 1 and 9 are the independent claims, and claims 1, 3-6, 8, 9, 11-14 and 16 are pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

Claims 1, 3-6, 8, 9, 11-14 and 16 were rejected under 35 USC §103(a) as obvious over *Nathanson* (US 5,969,385) in view of *Yamazaki* (US 2002/0109185 A1). This rejection is respectfully traversed.

An important object of the present invention is to control OFF-state leakage current without unduly reducing ON-state current. This is described in page 12, lines 26-32 of the specification, for example:

> As described above, in the first embodiment, when a gate electrode is made of P^+-type polysilicon, a channel is N-type, the N-type impurity concentration in the channel is approximately 3×10^{17} cm^{-3}, a gate length is 0.15 μm, and a gate threshold voltage becomes 0.36 V. As a result, a normalized OFF-state leakage current I_{off}/W is reduced to a desired value, and too small ON-state current can be avoided.

To attain this object, Applicant has found that the semiconductor device of the present invention must satisfy all of the following conditions (1) to (3), each of which is recited in both independent claims 1 and 9:

(1) the conductivity type of the gate electrode is P-type, and the conductivity type of the channel is N-type;

(2) the "impurity concentration in said channel is within a range approximately from 1×10^{17} cm^{-3} to 1×10^{18} cm^{-3}"; and

(3) "a channel length of said channel is within a range approximately from 0.1 μm to 0.25 μm".

There are two types of electrical charge carriers that move in the semiconductor layer, namely, electrons and holes in accordance with the conductivity types of the semiconductor layer. The speeds of movement of the electrons and the holes are different from each other.

Therefore, in the present invention, the object of which is to control OFF-state leakage current and ON-state current that are equivalent to the movement of electrical charge carriers, the conductivity types of the semiconductor layers constitute an important condition for achieving the above object.

This is described in the specification, for example, in page 8, lines 7-10:

> As can be understood from the curve T0 in FIG. 3 indicating a case where the N-type impurity concentration in the channel is approximately zero, a gate threshold voltage is approximately 0.73 V when the gate length is approximately 0.4 μm or more.

Page 8, lines 26-29:

> As can be understood from FIG. 3, a gate threshold voltage can be decreased by increasing the N-type impurity concentration in the channel, that is, a gate threshold voltage can be adjusted by controlling the N-type impurity concentration in the channel.

And page 9, lines 7-10:

> In the first embodiment, since the gate electrode is made of P^+-type polysilicon, the channel of the SOI film **103** is N-type, and a gate threshold voltage is approximately 0.36 V, a normalized OFF-state leakage current I_{off}/W can be suppressed.

The conditions set by features (1), (2) and (3) are therefore each necessary to achieve the above important objective of the invention, that is they act together in synergy to achieve the result of reducing the OFF-state leakage current while avoiding too low an ON-state current.

The Office Action alleges that *Nathanson* discloses the above-mentioned feature (1), ("said gate electrode is made of P-type polysilicon and conductivity types of said source, said drain and said channel are all N-type", lines 1-3, page 3 in the Office Action, referring to FIG. 3 of *Nathanson*) and the above-mentioned feature (3) ("[s]aid channel length of said channel is approximately 0.15 μm", at lines 6-7, page 3 in the Office action, referring to column 5 of *Nathanson*).

With respect to feature (1), *Nathanson* does <u>not</u> specify a <u>P-type</u> polysilicon gate. FIG. 3 of *Nathanson* shows two complementary transistors, one in which the source, drain and channel are N-type, and another in which they are P-type, but shows no polarity for the gate in either device. This is because *Nathanson*

primarily contemplates metal gate(s), which of course would not have any polarity, and notes only in the alternative that the gate(s) may be doped polysilicon (e.g. in the Summary of the Invention, column 2, lines 8-10: "As is known, doped polysilicon can be used in place of metal for the electrodes, including the gate electrode"), whilst remaining entirely silent on the polarity of any such doping, i.e. not specifying P-type.

Further, the Office Action admits that *Nathanson* does not disclose the above-mentioned feature (2) and alleges that this is disclosed by *Yamazaki* ("the area under the gate/channel has an impurity concentration ranging from 2 X 10^{16} to 5 X $10^{19}/cm^3$", at lines 13-14, page 3 in the Office Action, referring to Embodiment 1 and FIG. 2A-5B of *Yamazaki*).

Each of *Nathanson* and Yamazaki relate to MOS transistors. However, neither *Nathanson* nor *Yamazaki* teach or suggest that the technology disclosed in *Yamazaki* (i.e., *Yamazaki*'s impurity concentrations) can be used in the technology disclosed in *Nathanson* (i.e., in *Nathanson*'s device). Furthermore, the objects of *Nathanson* and *Yamazaki* are different from each other, and are also different from the object of the present invention. The object of *Nathanson* is to provide a semiconductor device with higher operational speed and lower power consumption, as shown in column 1, lines 40-48 in *Nathanson*, which is different from the object of the present invention.

Moreover, the object of *Yamazaki* is to provide a semiconductor device with lower OFF current, but not to control ON-state current. As discussed, this cannot be achieved when only some of the necessary conditions (1), (2) and (3) are met.

Consequently, one skilled in the art would not have been motivated to employ the impurity concentration of *Yamazaki* in the device of *Nathanson* to achieve the result of reducing the OFF-state leakage current and avoiding too low an ON-state current, as this would require impermissible hindsight.

The Office Action alleges, e.g. at page 3, lines 17-20 thereof, that using *Yamazaki*'s impurity concentrations in *Nathanson*'s device would "allow for better conductivity/device speed and allow the FET to vary the threshold voltage". Although it is axiomatic that a higher impurity concentration corresponds to a higher conductivity, there is no explanation as to why one of ordinary skill in the art would seek to increase the channel conductivity in the device of *Nathanson*, and it is not necessarily apparent that a device with a more heavily doped channel would always be faster. Nor is it clear what is meant by "allow the FET to vary the threshold voltage". Perhaps this should read "allow the threshold voltage of the FET to be varied", but there is no explanation of how or why the threshold voltage would or could be varied or why this might be desirable in the device of *Nathanson*.

Therefore, it would not have been obvious to one of ordinary skill in the art to make the present invention by combining *Nathanson* and *Yamazaki*.

In addition, neither *Nathanson* nor *Yamazaki* discloses a gate electrode "made of P-type polysilicon" as recited in both claim 1 and 9, such that if these references were to be combined, the combination would not anticipate all elements of the claimed invention.

Accordingly, the presently claimed invention is novel and not obvious over *Nathanson* and *Yamazaki*, whether taken as a whole or separately, and claims 1 and 9 are allowable, together with all claims that depend therefrom.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Should any fee be required, however, the Commissioner is hereby authorized to charge the fee to our Deposit Account No. 18-0002, and advise us accordingly.

Respectfully submitted,

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Date

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